ANNA UNIVERSITY, CHENNAI
NON- AUTONOMOUS COLLEGES AFFILIATED ANNA UNIVERSITY
M.E. VLSI DESIGN

REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM

1. PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

- To critically analyse and understand the principles involved in the designing and testing of electronic circuits relevant to industry and society.
- To appreciate the concepts in the working of electronic circuits.
- To take up socially relevant and challenging projects and to provide Innovative solutions through research for the benefit of the society with latest hardware & software related to VLSI and also to develop the capacity to protect Intellectual Property.
- To Progress and Develop with Ethics and Communicate effectively.
- To become entrepreneurs to develop indigenous solutions.

2. PROGRAM SPECIFIC OUTCOMES (PSOs) :

At the end of this program, the students will be able to

- Understand the fundamentals involved in the Designing and Testing of electronic circuits in the VLSI domain.
- Provide solutions through research to socially relevant issues for modern Electronic Design Automation (EDA) tools with knowledge, techniques, skills and for the benefit of the society.
- Interact effectively with the technical experts in industry and society.

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I TO IV SEMESTERS CURRICULA AND 1st SEMESTER SYLLABI
SEMESTER I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4153	Graph Theory and Optimization Techniques	FC	3	1	0	4	4
2.	RM4151	Research Methodology and IPR	RMC	2	0	0	2	2
3.	VL4151	Analog IC Design	PCC	3	0	0	3	3
4.	VL4152	Digital CMOS VLSI Design	PCC	3	0	0	3	3
5.	AP4152	Advanced Digital System Design	PCC	3	0	2	5	4
6.	AP4153	Semiconductor Devices and Modeling	PCC	3	0	0	3	3
7.		Audit Course – I*	AC	2	0	0	2	0
PRACTICALS								
8.	VL4111	FPGA Laboratory	PCC	0	0	4	4	2
9.	VL4112	Analog IC Design Laboratory	PCC	0	0	4	4	2
			TOTAL	**19**	**1**	**10**	**30**	**23**

*Audit course is optional

SEMESTER II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4251	Design for Verification using UVM	PCC	3	0	0	3	3
2.	VL4252	Low Power VLSI Design	PCC	3	0	0	3	3
3.	VL4253	RFIC Design	PCC	3	0	0	3	3
4.	VL4254	VLSI Testing	PCC	3	0	0	3	3
5.		Professional Elective I	PEC	3	0	0	3	3
6.		Professional Elective II	PEC	3	0	0	3	3
7.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
8.	VL4211	Verification using UVM Laboratory	PCC	0	0	4	4	2
9.	VL4212	Term Paper and Seminar	EEC	0	0	2	2	1
			TOTAL	**20**	**0**	**6**	**26**	**21**

*Audit course is optional

SEMESTER III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4351	VLSI Signal Processing	PCC	3	0	0	3	3
2.		Professional Elective III	PEC	3	0	0	3	3
3.		Professional Elective IV	PEC	3	0	2	5	4
4.		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
5.	VL4311	Project Work I	EEC	0	0	12	12	6
			TOTAL	**12**	**0**	**14**	**26**	**19**

SEMESTER IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICALS								
1.	VL4411	Project Work II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 75

PROFESSIONAL ELECTIVES

SEMESTER II, ELECTIVE I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4071	ASIC Design	PEC	3	0	0	3	3
2.	VE4152	Embedded System Design	PEC	3	0	0	3	3
3.	EL4071	Electromagnetic Interference and Compatibility	PEC	3	0	0	3	3
4.	VL4001	Data Converters	PEC	3	0	0	3	3
5.	VL4002	Hardware Software Co-Design for FPGA	PEC	3	0	0	3	3
6.	IF4078	Pattern Recognition	PEC	3	0	0	3	3

SEMESTER II, ELECTIVE II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4003	DSP Structures for VLSI	PEC	3	0	0	3	3
2.	VL4004	Power Management and Clock Distribution Circuits	PEC	3	0	0	3	3
3.	VL4005	Reconfigurable Architectures	PEC	3	0	0	3	3
4.	VL4006	Advanced Wireless Sensor Networks	PEC	3	0	0	3	3
5.	AP4078	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
6.	II4072	System On Chip	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4073	MEMS and NEMS	PEC	3	0	0	3	3
2.	VL4074	Network on Chip	PEC	3	0	0	3	3
3.	CU4075	VLSI for Wireless Communication	PEC	3	0	0	3	3
4.	VL4075	Nanotechnology	PEC	3	0	0	3	3
5.	VL4007	Evolvable Hardware	PEC	3	0	0	3	3
6.	AP4079	Soft Computing and Optimization Techniques	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4008	VLSI Architectures for Image Processing	PEC	3	0	2	5	4
2.	VL4009	CAD for VLSI Design	PEC	3	0	2	5	4
3.	VL4010	System Verilog	PEC	3	0	2	5	4
4.	VL4011	Adaptive Signal Processing	PEC	3	0	2	5	4
5.	CP4252	Machine Learning	PEC	3	0	2	5	4
6.	DS4151	Digital Image and Video Processing	PEC	3	0	2	5	4

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			L	T	P	
1.	AX4091	English for Research Paper Writing	2	0	0	0
2.	AX4092	Disaster Management	2	0	0	0
3.	AX4093	Constitution of India	2	0	0	0
4.	AX4094	நற்றமிழ் இலக்கியம்	2	0	0	0

VL4153 GRAPH THEORY AND OPTIMIZATION TECHNIQUES L T P C
3 1 0 4

COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real life situation.
- To provide knowledge and training using non-linear programming under limited resources for engineering and business problems.
- To understand the applications of simulation modelling in engineering problems.

UNIT I GRAPHS 12

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II GRAPH ALGORITHM 12

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT IV NON-LINEAR PROGRAMMING 12

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT V SIMULATION MODELLING 12

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

- apply graph ideas is solving connectivity related problems.
- apply fundamental graph algorithms to solve certain optimization problems.
- formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
- model various real life situations as optimization problems and effect their solution through Non-linear programming.
- apply simulation modeling techniques to problems drawn from industry management and other engineering fields.

TEXT BOOKS:

1. Taha H.A, “Operation Research: An Introduction”, Ninth Edition, Pearson Education, New Delhi, 2010.
2. Gupta P. K, and Hira D.S., “Operation Research”, Revise Edition, S. Chand and Company Ltd., 2012.

3. Sharma J.K., “Operation Research”, 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, “Introduction to Graph Theory”, Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., “ A text book of Graph Theory”, Springer Science and Business Media, New Delhi, 2012.
6. Narasingh Deo, “Graph Theory with Applications to Engineering and Computer Science”, Prentice Hall India,1997.

RM4151 RESEARCH METHODOLOGY AND IPR L T P C
2 0 0 2

UNIT I RESEARCH DESIGN 6

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES 6

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING 6

Overview of Multivariate analysis, Hypotheses testing and Measures of Association.
Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS 6

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V PATENTS 6

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL:30 PERIODS

REFERENCES:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
3. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

VL4151 **ANALOG IC DESIGN** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- Analog Circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog IC will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER 9

Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.

UNIT V BANDGAP REFERENCES 9

Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: Design amplifiers to meet user specifications
CO2: Analyse the frequency and noise performance of amplifiers
CO3: Design and analyse feedback amplifiers and one stage op amps
CO4: Design and analyse two stage op amps
CO5: Design and analyse current mirrors and current sinks with mos devices

TOTAL: 45 PERIODS

REFERENCES

1. Behzad Razavi, “Design Of Analog Cmos Integrated Circuits”, Tata Mcgraw Hill, 2001.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.
3. Grebene, “Bipolar And Mos Analog Integrated Circuit Design”, John Wiley & Sons,Inc.,2003.
4. Phillip E.Allen, Douglas R .Holberg, “Cmos Analog Circuit Design”, Oxford University Press, 2nd Edition, 2002.
5. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start
6. Jacob Baker “CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.

VL4152 DIGITAL CMOS VLSI DESIGN L T P C

3 0 0 3

COURSE OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V MEMORY ARCHITECTURES 6

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits

CO2: Create models of moderately sized static CMOS combinational circuits that realize

specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort

CO3: Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches

CO4: Understand design methodology of arithmetic building blocks

CO5: Design functional units including ROM and SRAM

REFERENCES:

1. N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993
2. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
3. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998
4. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

AP4152 ADVANCED DIGITAL SYSTEM DESIGN L T P C

3 0 2 4

COURSE OBJECTIVES:

- To design asynchronous sequential circuits.
- To learn about hazards in asynchronous sequential circuits.
- To study the fault testing procedure for digital circuits.
- To understand the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment-Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method-Path Sensitization Method – Boolean Difference Method - D Algorithm — Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming Logic Device Families – Designing a Synchronous Sequential Circuit using PLA/PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA – Xilinx FPGA - Xilinx 4000.

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types And Operators For Modelling In Verilog HDL - Behavioural Descriptions In Verilog HDL – HDL Based Synthesis – Synthesis

Of Finite State Machines– Structural Modelling – Compilation And Simulation Of Verilog Code – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog – Registers – Counters – Sequential Machine – Serial Adder – Multiplier- Divider – Design Of Simple Microprocessor, Introduction To System Verilog.

45 PERIODS

SUGGESTED ACTIVITIES:

1: Design asynchronous sequential circuits.
2: Design synchronous sequential circuits using PLA/PAL.
3: Simulation of digital circuits in FPGA.
4: Design digital systems with System Verilog.

PRACTICAL EXERCISES: **30 PERIODS**

1. Design of Registers by Verilog HDL.
2. Design of Counters by Verilog HDL.
3. Design of Sequential Machines by Verilog HDL.
4. Design of Serial Adders , Multiplier and Divider by Verilog HDL.
5. Design of a simple Microprocessor by Verilog HDL.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Analyse and design synchronous sequential circuits.
CO2: Analyse hazards and design asynchronous sequential circuits.
CO3: Knowledge on the testing procedure for combinational circuit and PLA.
CO4: Able to design PLD and ROM.
CO5: Design and use programming tools for implementing digital circuits of industry standards.

TOTAL:75 PERIODS

REFERENCES:

1. Charles H.Roth jr., “Fundamentals of Logic Design” Thomson Learning,2013.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
5. Paragk.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
6. Paragk.Lala “Digital System Design Using PLD” B S Publications,2003.
7. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

AP4153 **SEMICONDUCTOR DEVICES AND MODELING** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.
- To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications
- To acquire the fundamental knowledge of different semiconductor device modelling aspects.

UNIT I MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–OxideInterface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT II MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III CMOS DEVICE DESIGN 9

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT IV BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.

UNIT V MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, the students will be able to

CO1: Explore the properties of MOS capacitors.

CO2: Analyze the various characteristics of MOSFET devices.

CO3: Describe the various CMOS design parameters and their impact on performance of the device.

CO4: Discuss the device level characteristics of BJT transistors.

CO5: Identify the suitable mathematical technique for simulation.

REFERENCES:

1. Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.
2. A.B. Bhattacharyya “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Ltd, 2009.
3. Ansgar Jungel, “Transport Equations for Semiconductors”, Springer, 2009
4. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2004
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
6. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition, 2014
7. J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer, 2002.
8. S.M.Sze, Kwok.K. NG, “Physics of Semiconductor devices”, Springer, 2006.

VL4111 FPGA LABORATORY L T P C

0 0 4 2

COURSE OBJECTIVES:

- To help engineers read, understand, and maintain digital hardware models and conventional verification test benches written in Verilog and System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog

LIST OF EXPERIMENTS

1. Introduction to Verilog and System Verilog
2. Running simulator and debug tools
3. Experiment with 2 state and 4 state data types
4. Experiment with blocking and non-blocking assignments
5. Model and verify simple ALU
6. Model and verify an Instruction stack
7. Use an interface between testbench and DUT
8. Developing a test program
9. Create a simple and advanced OO testbench
10. Create a scoreboard using dynamic array
11. Use mailboxes for verification
12. Generate constrained random test values
13. Using coverage with constrained random tests

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Understand and use the System Verilog RTL design and synthesis features, including new data types, literals, procedural blocks, statements, and operators, relaxation of Verilog language rules, fixes for synthesis issues, enhancements to tasks and functions, new hierarchy and connectivity features, and interfaces.

CO2: Appreciate and apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification.

CO3: The implementation of higher level of abstraction to design and verification

CO4: Develop Verilog test environments of significant capability and complexity.

CO5: Integrate scoreboards, multichannel sequencers and Register Models

VL4112 **ANALOG IC DESIGN LABORATORY** **L T P C**
0 0 4 2

COURSE OBJECTIVES:

- Carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, exposure to state of art CAD VLSI tool in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

LIST OF EXPERIMENTS

1. Extraction of process parameters of CMOS process transistors
   a. Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS.
   b. Plot I_D vs. V_{GS} at particular drain voltage for NMOS, PMOS and determine Vt.
   c. Plot log I_D vs. VGS at particular gate voltage for NMOS, PMOS and determine I_{OFF} and sub-threshold slope.
   d. Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use V_{DS} of appropriate voltage To extract V_{th} use the following procedure.
      i. Plot g_m vs V_{GS} using SPICE and obtain peak g_m point.
      ii. Plot $y=I_D/(g_m)$ as a function of VGS using SPICE.
      iii. Use SPICE to plot tangent line passing through peak gm point in y (V_{GS}) plane and determine V_{th}.
   f. Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.

2. CMOS inverter design and performance analysis
   a. i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine transition voltage and gain g. Calculate V_{IL}, V_{IH}, NM_H, NM_L for the inverter.
   ii. Plot VTC for CMOS inverter with varying V_{DD}.
   iii. Plot VTC for CMOS inverter with varying device ratio.
   b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay t_{pHL}, t_{pLH}, 20%-to-80% rise time t_r and 80%-to-20% fall time t_f.
   c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis
   a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve $V_{DSQ}=V_{DD}/2$.
      ii. Calculate input bias voltage for a given bias current.

iii. Use spice and obtain the bias current. Compare with the theoretical value
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
v. using small signal analysis in spice, considering load capacitance.
vi. Plot step response of the amplifier with a specific input pulse amplitude.
vii. Derive time constant of the output and compare it with the time constant
viii. resulted from -3dB Band Width.
ix. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier (INA).

Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.
ii. Draw the schematic of INA.
iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:
i.low-frequency voltage gain,

ii.unity gain BW (fu),

iii.input capacitance,

iv.output resistance,

v.CMRR

d. Draw schematic diagram of CMRR simulation setup.

e. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

f. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

g. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.

a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.
b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
c. Extract the netlist. Use extracted netlist and obtain $t_{PHL}t_{PLH}$ for the inverter using Spice.
d. Use a specific interconnect length and connect and connect three inverters in a chain.
e. Extract the new netlist and obtain t_{PHL} and t_{PLH} of the middle inverter.
f. Compare new values of delay times with corresponding values obtained in part ‘c’.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter

a. low-frequency voltage gain,
b. unity gain BW (fu),
c. Power dissipation

i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
ii. Perform time domain simulation and verify low frequency gain.
iii. Perform AC analysis and verify.

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design digital and analog Circuit using CMOS given a design specification.

CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO3: Use EDA tools for Circuit Design

AUDIT COURSES

AX4091 ENGLISH FOR RESEARCH PAPER WRITING **L T P C**
2 0 0 0

COURSE OBJECTIVES:

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING **6**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS **6**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS **6**

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS **6**

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS **6**

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES:

CO1 –Understand that how to improve your writing skills and level of readability

CO2 – Learn about what to write in each section

CO3 – Understand the skills needed when writing a Title

CO4 – Understand the skills needed when writing the Conclusion

CO5 – Ensure the good quality of paper at very first-time submission

REFERENCES:

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

AX4092 DISASTER MANAGEMENT L T P C
2 0 0 0

COURSE OBJECTIVES:

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS

COURSE OUTCOMES:

CO1: Ability to summarize basics of disaster

CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5: Ability to develop the strengths and weaknesses of disaster management approaches

REFERENCES:

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company,2007.
3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

AX4093 CONSTITUTION OF INDIA L T P C
2 0 0 0

COURSE OBJECTIVES:

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION

History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION

Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila

Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING

1. The Constitution of India,1950(Bare Act),Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AX4094 **நற்றமிழ் இலக்கியம்** **L T P C**
2 0 0 0

UNIT I **சங்க இலக்கியம்** **6**

1. தமிழின் துவக்க நூல் தொல்காப்பியம்
   – எழுத்து, சொல், பொருள்
2. அகநானூறு (82)
   - இயற்கை இன்னிசை அரங்கம்
3. குறிஞ்சிப் பாட்டின் மலர்க்காட்சி
4. புறநானூறு (95,195)
   - போரை நிறுத்திய ஔவையார்

UNIT II **அறநெறித் தமிழ்** **6**

1. அறநெறி வகுத்த திருவள்ளுவர்
   - அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புறவு அறிதல், ஈகை, புகழ்
2. பிற அறநூல்கள் - இலக்கிய மருந்து
   – ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)

UNIT III **இரட்டைக் காப்பியங்கள்** **6**

1. கண்ணகியின் புரட்சி
   - சிலப்பதிகார வழக்குரை காதை
2. சமூகசேவை இலக்கியம் மணிமேகலை
   - சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை

UNIT IV **அருள்நெறித் தமிழ்** **6**

1. சிறுபாணாற்றுப்படை
   - பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள்
2. நற்றிணை
   - அன்னைக்குரிய புன்னை சிறப்பு
3. திருமந்திரம் (617, 618)
   - இயமம் நியமம் விதிகள்
4. தர்மச்சாலையை நிறுவிய வள்ளலார்
5. புறநானூறு
   - சிறுவனே வள்ளலானான்
6. அகநானூறு (4) - வண்டு
   நற்றிணை (11) - நண்டு
   கலித்தொகை (11) - யானை, புறா
   ஐந்தினை 50 (27) - மான்

ஆகியவை பற்றிய செய்திகள்

UNIT V **நவீன தமிழ் இலக்கியம்** **6**

1. உரைநடைத் தமிழ்,
   - தமிழின் முதல் புதினம்,
   - தமிழின் முதல் சிறுகதை,
   - கட்டுரை இலக்கியம்,
   - பயண இலக்கியம்,
   - நாடகம்,
2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும்,
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும்,
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும்,
5. அறிவியல் தமிழ்,
6. இணையத்தில் தமிழ்,
7. சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.

TOTAL: 30 PERIODS

<u>தமிழ் இலக்கிய வெளியீடுகள் / புத்தகங்கள்</u>

1. தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University)

- www.tamilvu.org
2. தமிழ் விக்கிப்பீடியா (Tamil Wikipedia)
-https://ta.wikipedia.org
3. தர்மபுர ஆதின வெளியீடு
4. வாழ்வியல் களஞ்சியம்
- தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்
5. தமிழ்கலைக் களஞ்சியம்
- தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6. அறிவியல் களஞ்சியம்
- தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்